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| AIUB | **American International University- Bangladesh (AIUB)**  **Faculty of Engineering (FE)** | | | | | | | | | |
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| **Course Name :** | | Digital Logic & Circuits Laboratory | | | | | **Course Code :** | | EEE 1204 | |
| **Semester :** | | Fall 2024-25 | | | | | **Sec :** | | G | |
| **Lab Instructor :** | | MD. ALOMGIR KABIR | | | | | **Group :** | | 07 | |
|  | |  | | | | |  | |  | |
| **Experiment No :** | | 06 | | | | | | | | |
| **Experiment Name :** | | Construction of MOSFET Logic Gates | | | | | | | | |
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| **Submitted by (NAME):** | | **Chinmoy Guha** | | | | **Student ID:** | | | **22-48056-2** | |
|  | |  | | | |  | | |  | |
| **Group Members** | | | | | **ID** | | | **Name** | | |
|  | | | | 1. | 22-48056-2 | | | CHINMOY GUHA | | |
|  | | | | 2. | 22-48067-2 | | | SUVRA CHAKRABORTY | | |
|  | | | | 3. | 22-47975-2 | | | MOHAMMAD ANSAR UDDIN | | |
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| **Performance Date :** | | | **11/12/24** | | | **Due Date :** | | | | **08/01/25** |
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**Marking Rubrics (to be filled by Lab Instructor)**

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| --- | --- | --- | --- | --- | --- |
| Category | Proficient  [6] | Good  [4] | Acceptable  [2] | Unacceptable [1] | Secured Marks |
| **Theoretical Background, Methods  & procedures sections** | All information, measures and variables are provided and explained. | All Information provided that is sufficient, but more explanation is needed. | Most information correct, but some information may be missing or inaccurate. | Much information missing and/or inaccurate. |  |
| **Results** | All of the criteria are met; results are described clearly and accurately; | Most criteria are met, but there may be some lack of clarity and/or incorrect information. | Experimental results don’t match exactly with the theoretical values and/or analysis is unclear. | Experimental results are missing or incorrect; |  |
| **Discussion** | Demonstrates thorough and sophisticated understanding. Conclusions drawn are appropriate for analyses; | Hypotheses are clearly stated, but some concluding statements not supported by data or data not well integrated. | Some hypotheses missing or misstated; conclusions not supported by data. | Conclusions don’t match hypotheses, not supported by data; no integration of data from different sources. |  |
| **General formatting** | Title page, placement of figures and figure captions, and other formatting issues all correct. | Minor errors in formatting. | Major errors and/or missing information. | Not proper style in text. |  |
| **Writing & organization** | Writing is strong and easy to understand; ideas are fully elaborated and connected; effective transitions between sentences; no typographic, spelling, or grammatical errors. | Writing is clear and easy to understand; ideas are connected; effective transitions between sentences; minor typographic, spelling, or grammatical errors. | Most of the required criteria are met, but some lack of clarity, typographic, spelling, or grammatical errors are present. | Very unclear, many errors. |  |
| Comments: |  | | | Total Marks  (Out of ): |  |

**Abstract:**

**MOSFET Categories and Functionality:**  
MOSFETs are classified into four types: enhancement mode or depletion mode, and n-channel or p-channel. This discussion focuses solely on n-channel enhancement mode MOSFETs, which operate as voltage-controlled devices. Unlike current-driven bipolar transistors, these MOSFETs require a positive gate-to-source voltage (UGS) to create a conductive path between the source and drain. The applied voltage generates an electrostatic field, forming a channel that allows electrons to flow. Increasing the gate voltage enlarges the channel, enhancing current flow and demonstrating the principles of enhancement mode operation.

**Overview of CMOS Technology:**  
Complementary metal–oxide–semiconductor (CMOS) technology integrates n-channel and p-channel MOSFETs to create efficient digital and analog circuits. Invented by Frank Wanlass in 1963, CMOS is widely used in microprocessors, microcontrollers, static RAM, image sensors, and communication transceivers. Its design ensures only one transistor in a complementary pair conducts at a time, minimizing power consumption and heat generation while providing high noise immunity.

**Significance and Applications:**  
CMOS technology’s energy efficiency and ability to support high-density logic make it indispensable for very-large-scale integration (VLSI) chips. It has surpassed older technologies, such as transistor–transistor logic (TTL) and NMOS logic, in both performance and scalability, cementing its role in modern electronic systems.

**Objectives:**

Explore the construction and characterization of MOSFET logic gates.

 **Process:** Systematically assemble and analyze MOSFET-based logic gates.

 **Focus:** Investigate the functionality and performance of various gates, including:

* NAND gates
* NOR gates
* Basic logic gates

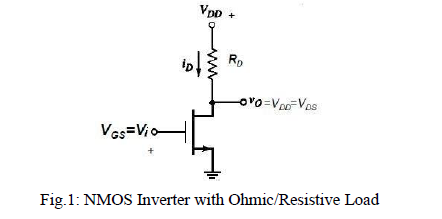
 **Goal:** Enhance understanding of MOSFET-based digital circuit design.

 **Applications:** Highlight the relevance of MOSFET logic gates in modern electronics.

**Theory and Methodology:**

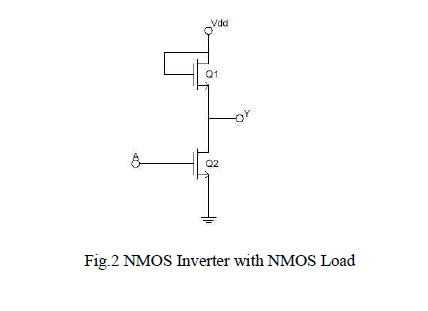
***NMOS Inverter with Ohmic/ Resistive Load:***

In an ideal situation, applying a HIGH voltage (+5V) to the input activates the NMOS transistor, allowing current to flow from Vdd to ground, resulting in an output voltage (Vo) of 0V. Conversely, when a LOW voltage (0V) is applied to the input, the NMOS transistor remains OFF, preventing current flow from Vdd to ground. Consequently, the output voltage is +5V.

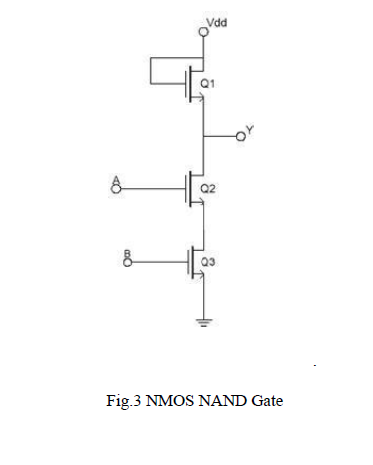


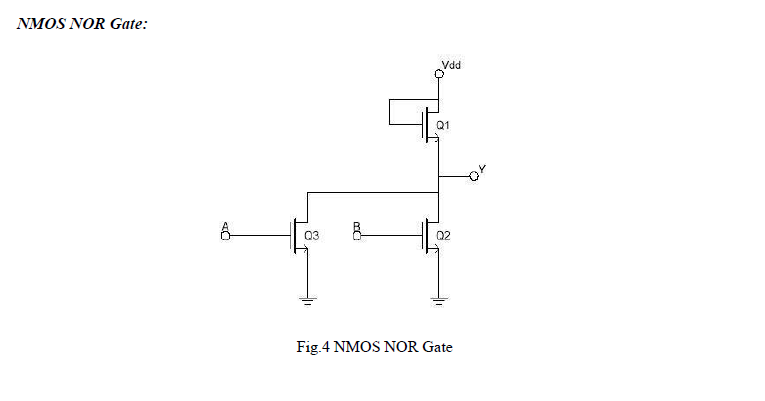
***NMOS Inverter with NMOS Enhancement Transistor load:***

A drawback of designing NMOS logic circuits with an ohmic load is the static power dissipation that occurs even when the NMOS transistor is OFF, due to the presence of the resistor. A more efficient design involves using an enhancement-type NMOS as the load. These transistors are "normally-off" devices, requiring a specific gate-to-drain voltage of the correct polarity to turn them ON. This approach effectively eliminates static power consumption.



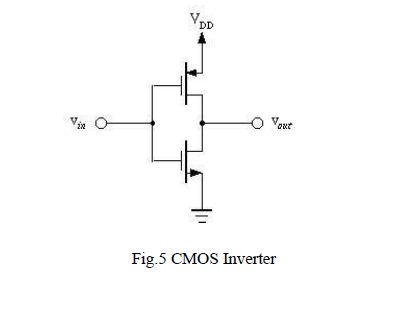
***NMOS NAND Gate:***

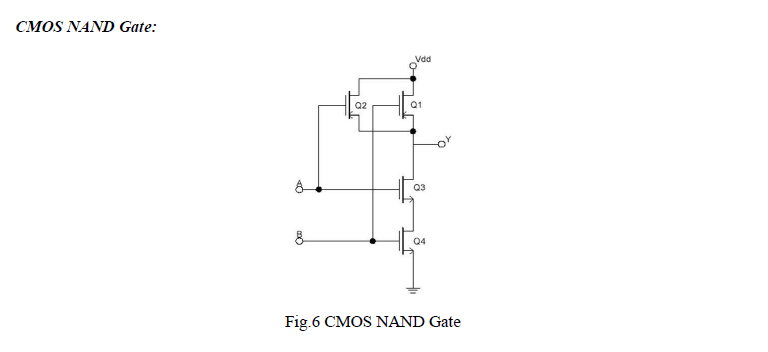


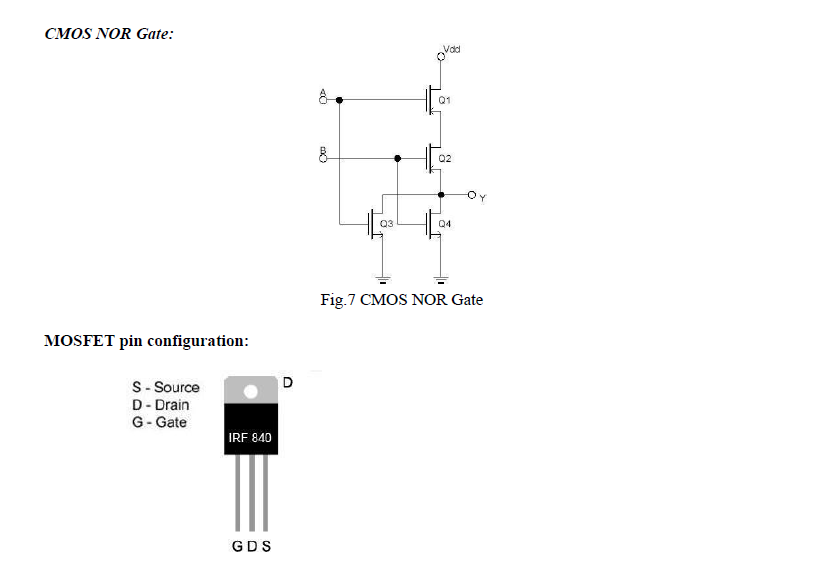


**CMOS Logic:**  
CMOS transistors are smaller and exhibit lower power dissipation compared to NMOS transistors, making them the preferred choice for integrated circuit designs across various applications. A CMOS configuration combines one p-channel MOSFET (PMOS) and one n-channel MOSFET (NMOS), designed with complementary characteristics. When OFF, these transistors have an effectively infinite resistance; when ON, their channel resistance is low (approximately 200 Ω). Since the gate acts as an open circuit, it does not draw current, and the output voltage corresponds to either ground or the power supply voltage, depending on which transistor is conducting.

**CMOS Inverter:**  
In a CMOS inverter, when the input is grounded (logic 0), the N-channel MOSFET remains unbiased and does not form a conductive channel, leaving the output line disconnected from ground. Simultaneously, the P-channel MOSFET is forward biased, creating a low-resistance channel (about 200 Ω) that connects the output line to the +V supply, resulting in an output of +V (logic 1).  
When the input is at +V (logic 1), the P-channel MOSFET turns OFF, while the N-channel MOSFET turns ON, pulling the output down to ground (logic 0). This configuration ensures correct logic inversion while providing active pull-up and pull-down functionality based on the output state.







**Apparatus used:**

(1) 10KΩ resistor (brown-black-orange).

(2) 1N914 diodes or equivalent.

**(3)** Connecting wires.

(4) Trainer Board

**Hardware Implementation and Simulation:**

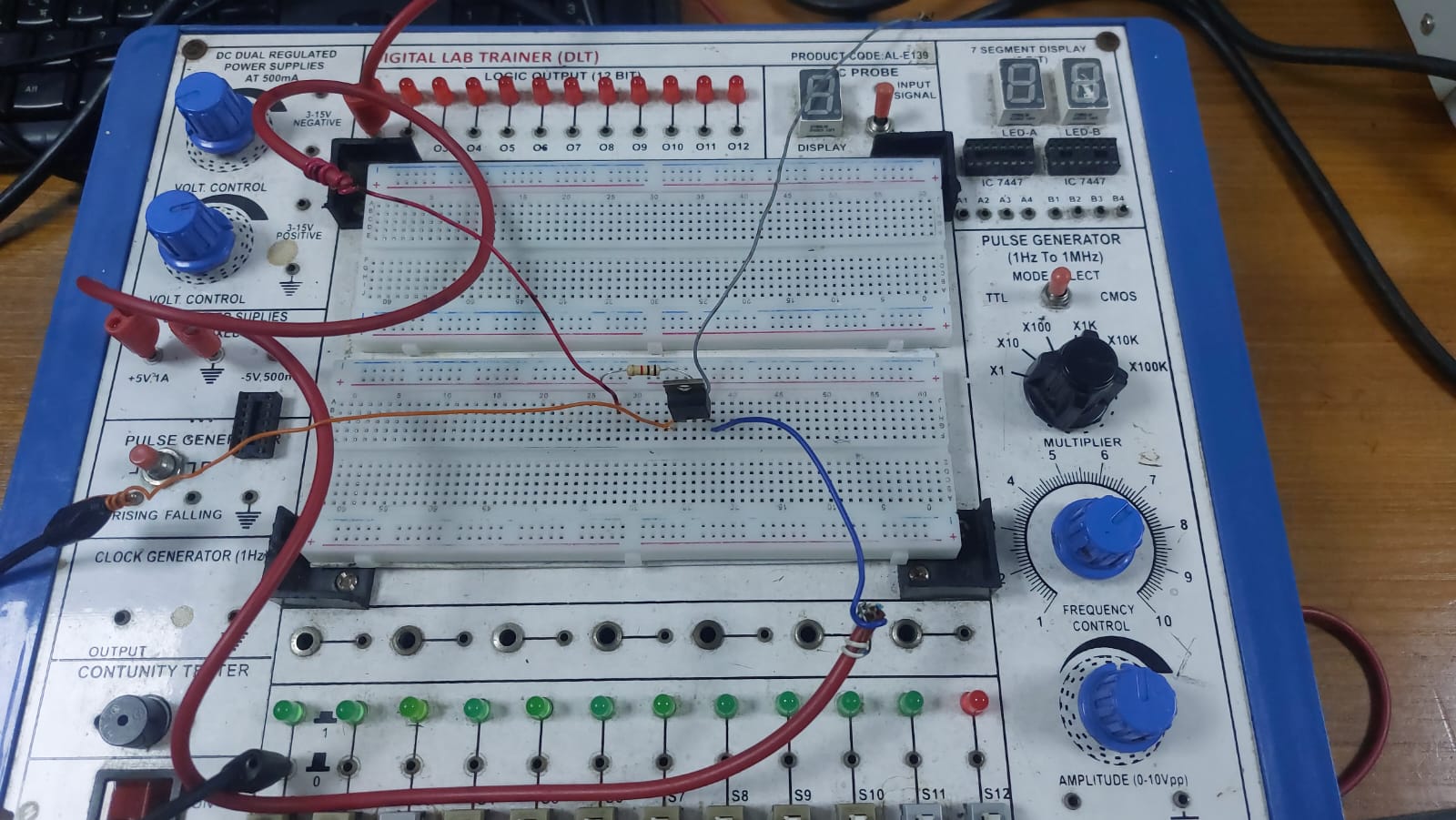
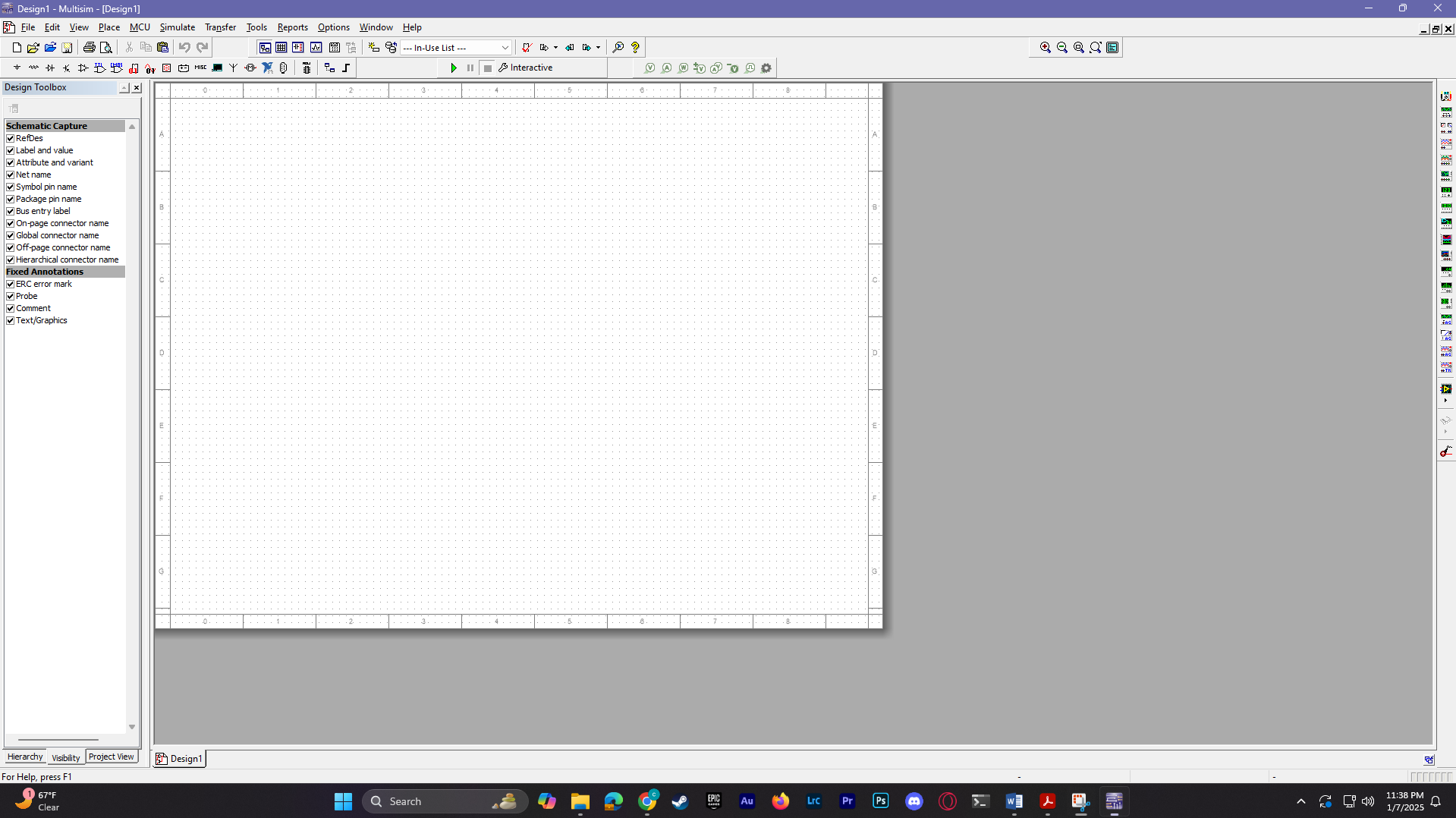
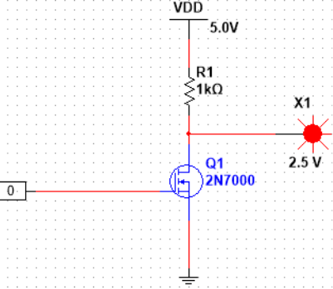


Fig.1: NMOS Inverter with Ohmic/Resistive Load



Simulation: NMOS Inverter with Ohmic/Resistive Load

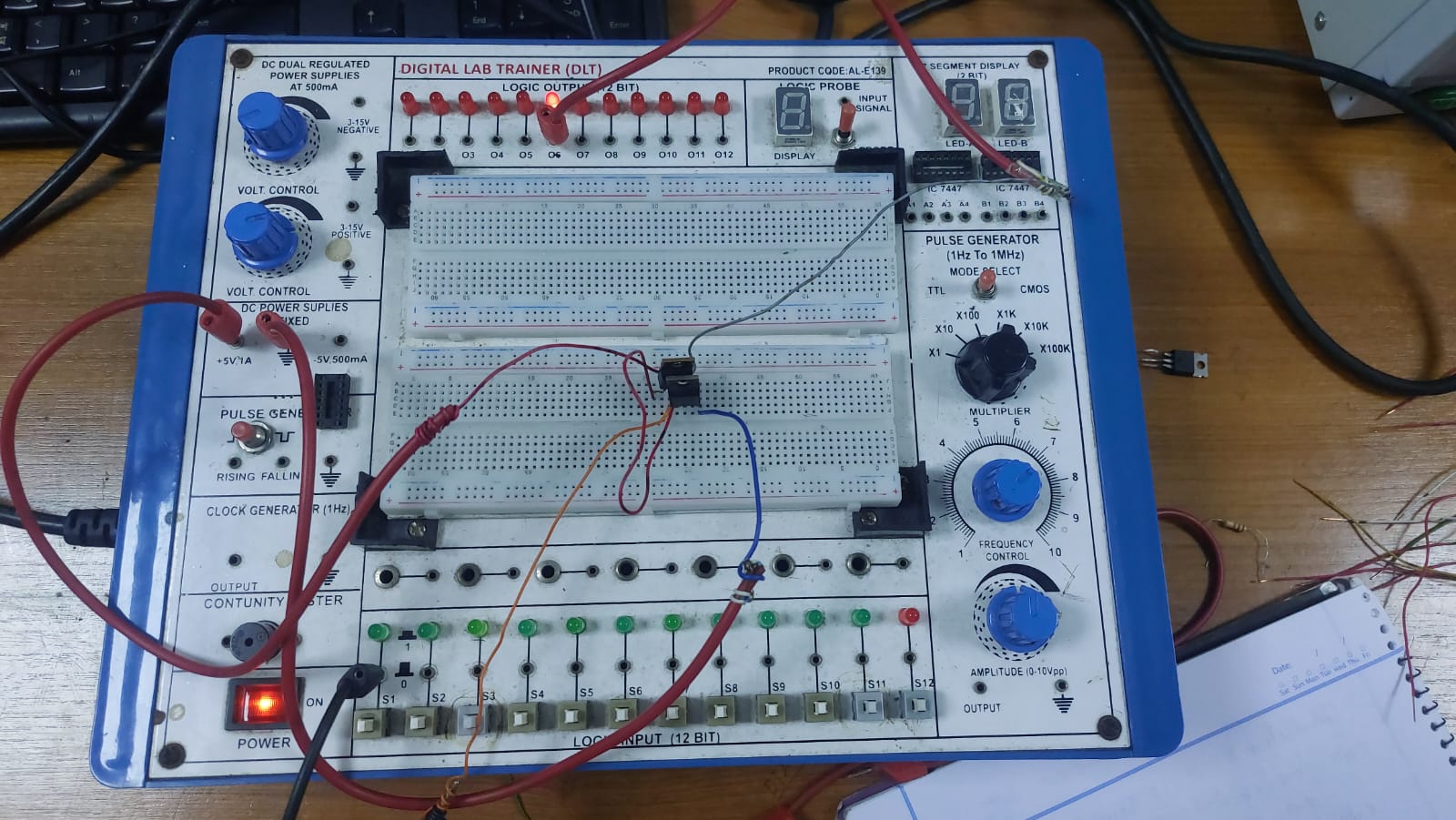
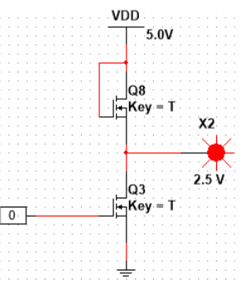
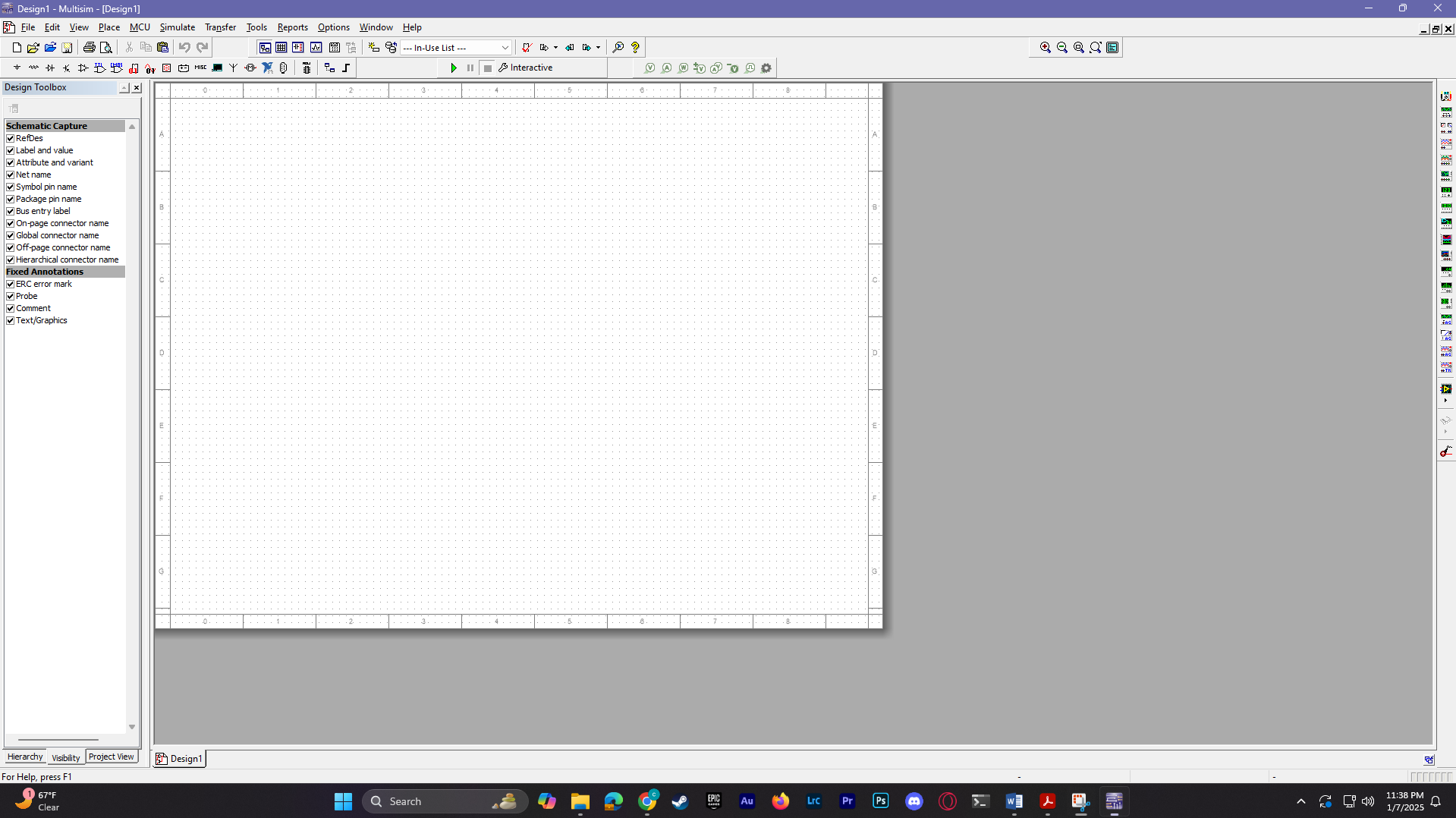


Fig.2 NMOS Inverter with NMOS Load

Simulation: NMOS Inverter with NMOS Load

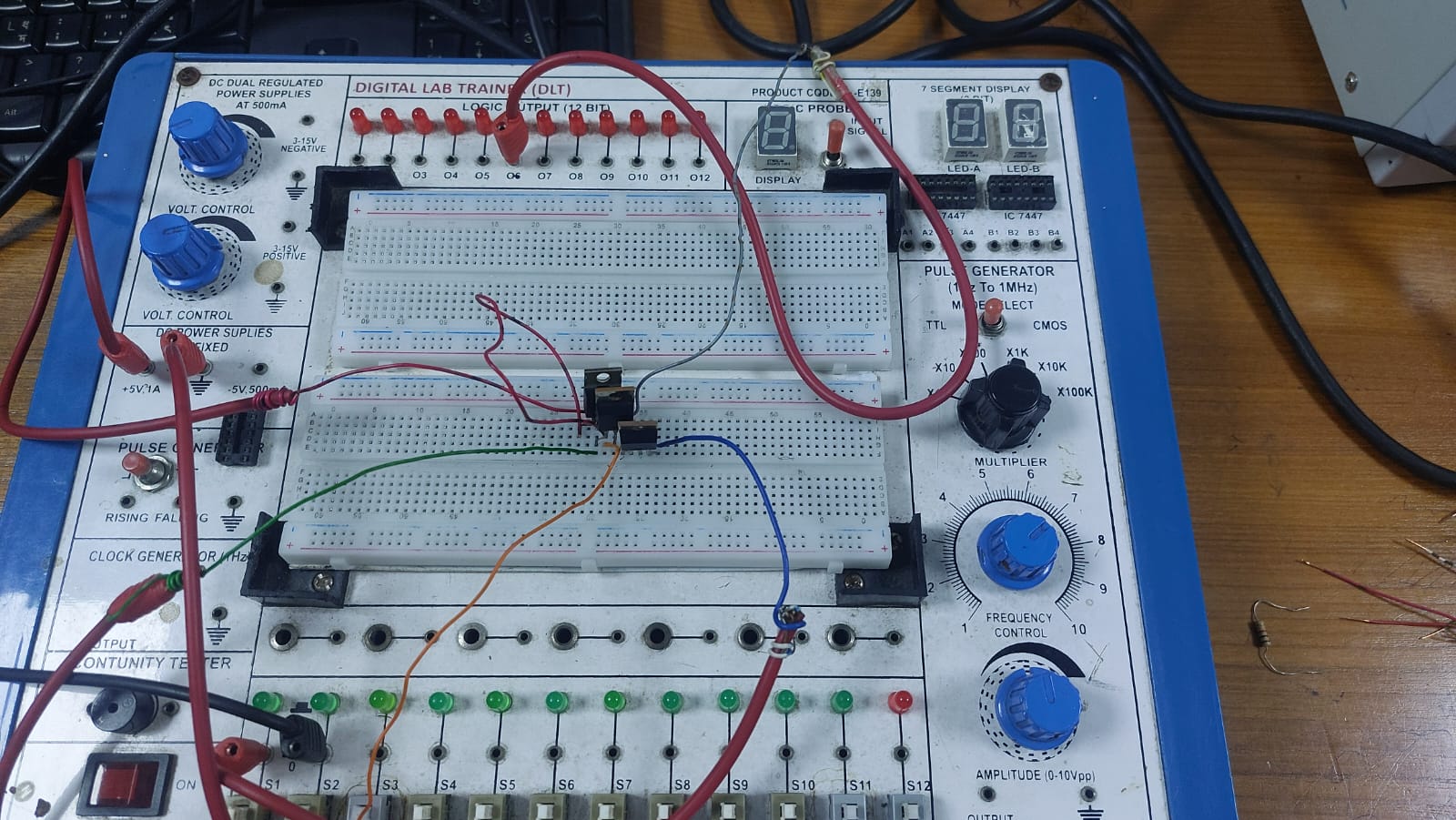
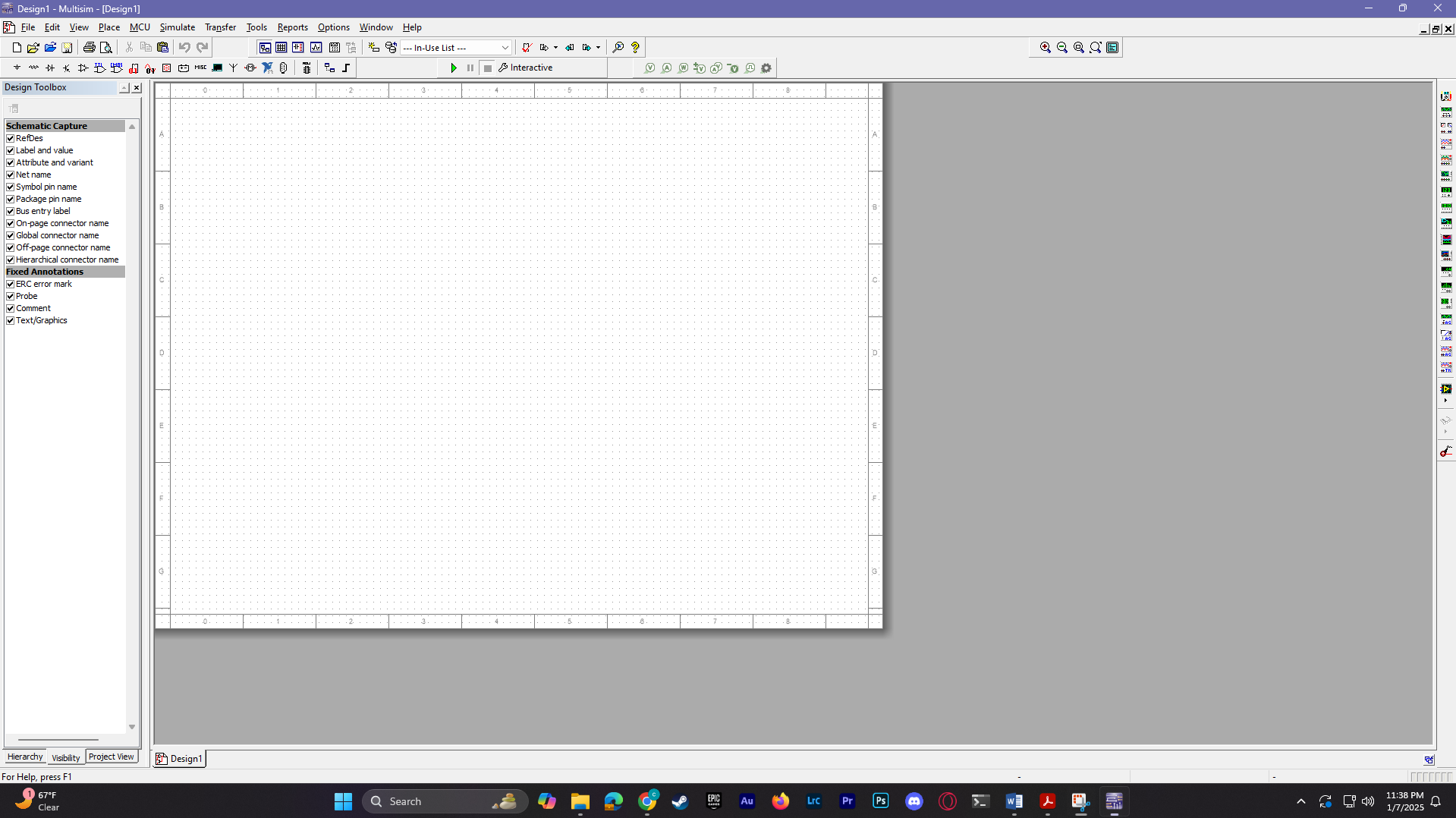
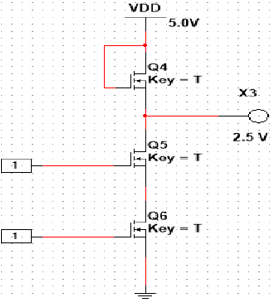


Fig.3 NMOS NAND Gate



Simulation: NMOS NAND Gate

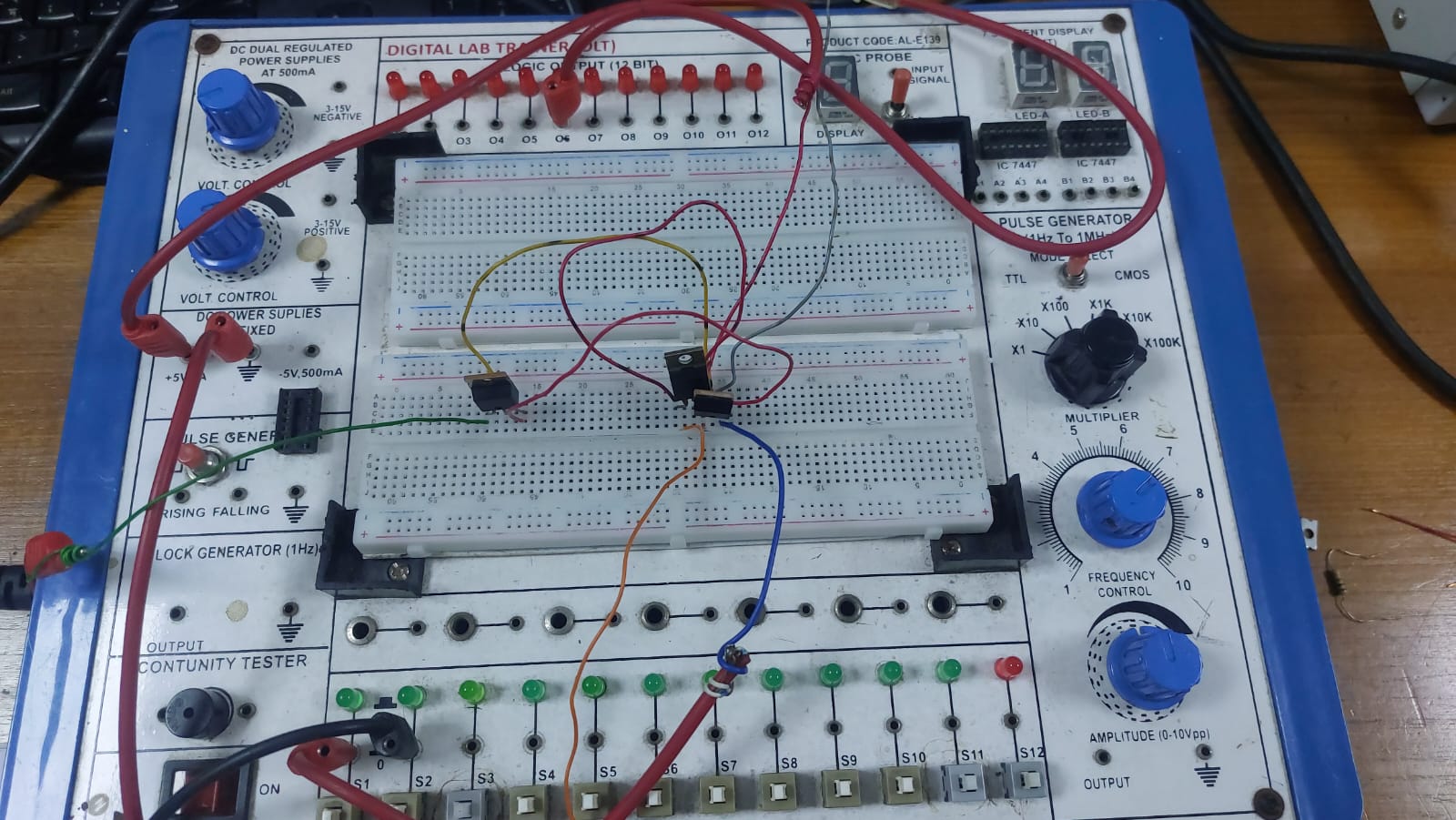
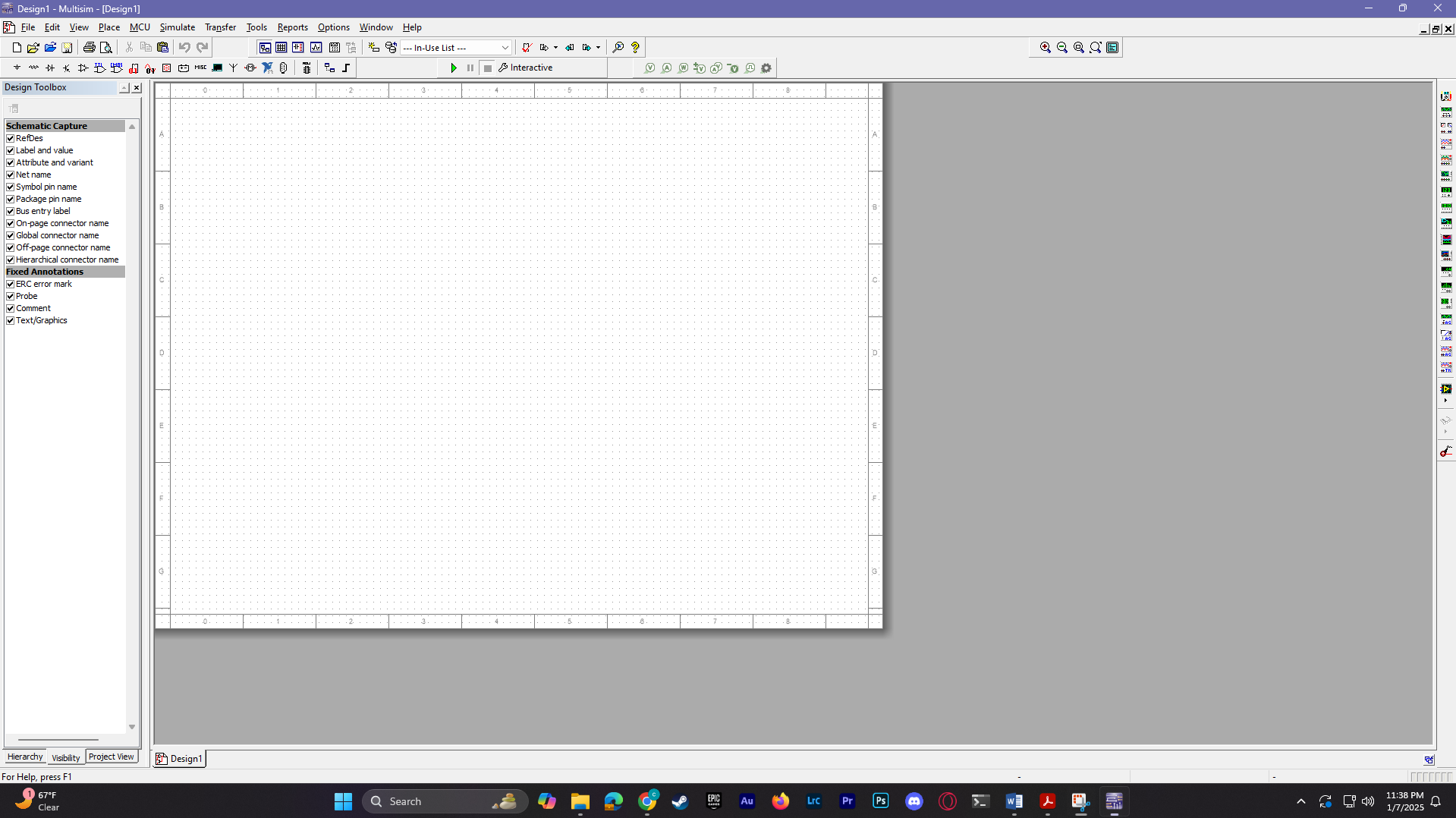
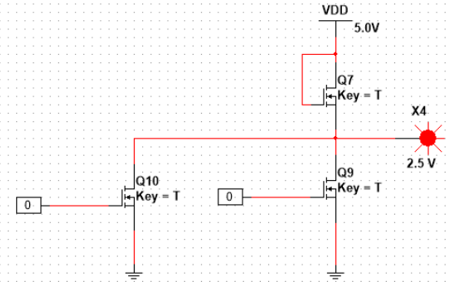


Fig.4 NMOS NOR Gate



Simulation: NMOS NOR Gate

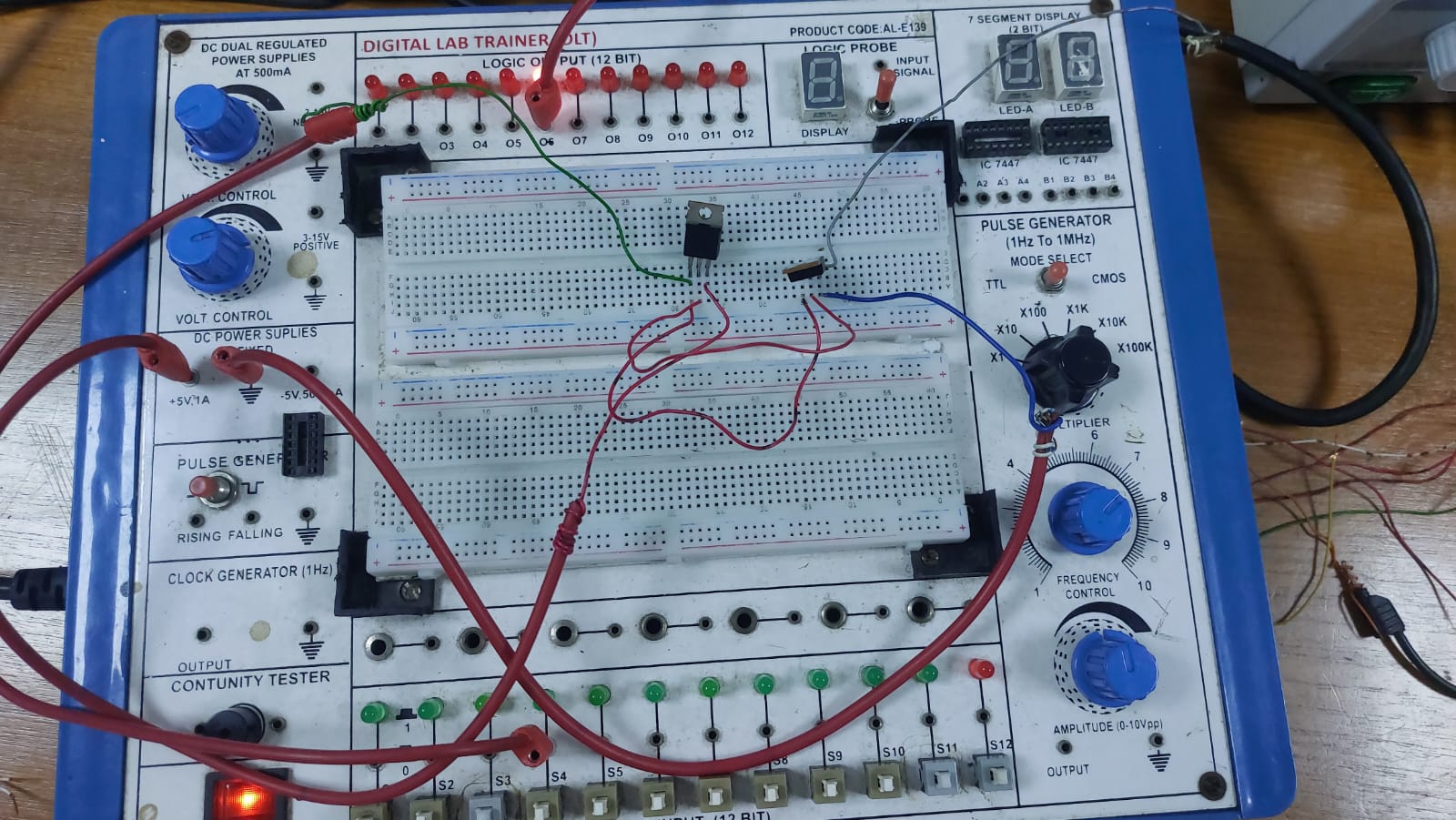
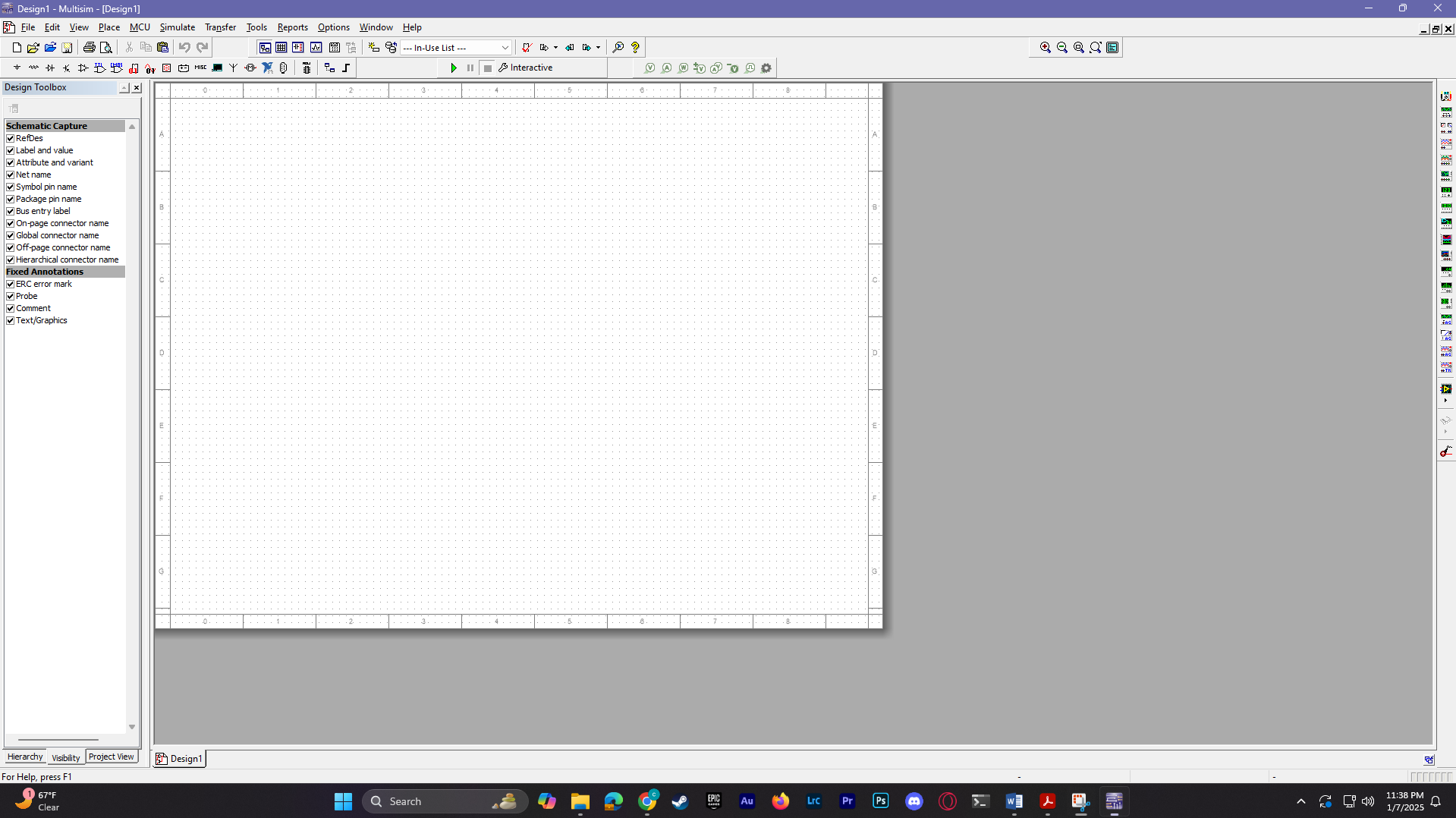
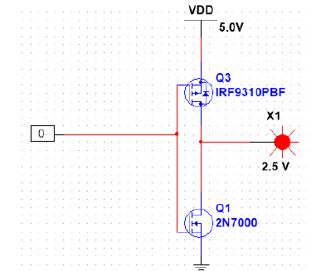


Fig.5 CMOS Inverter



Simulation: CMOS Inverter

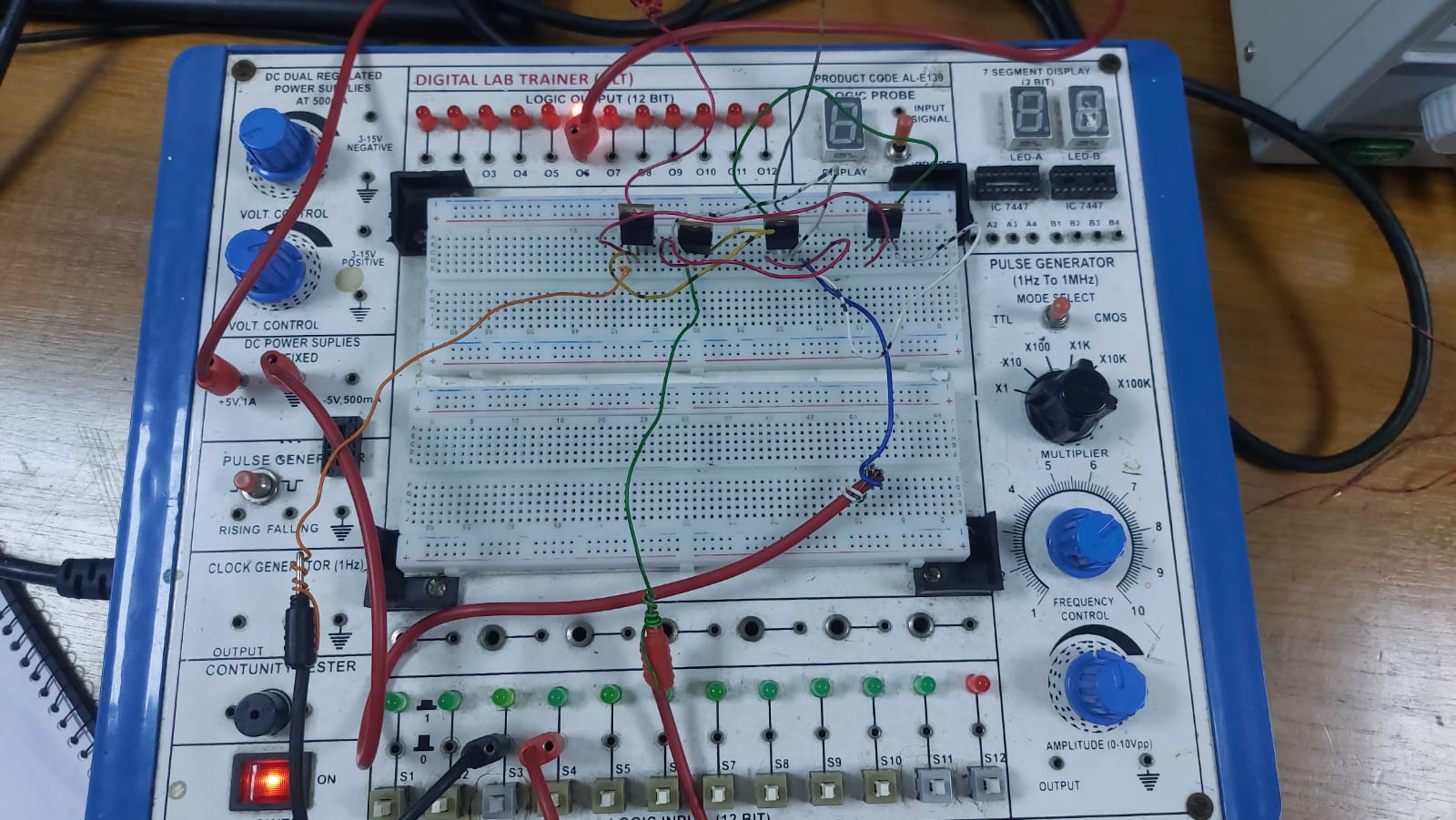
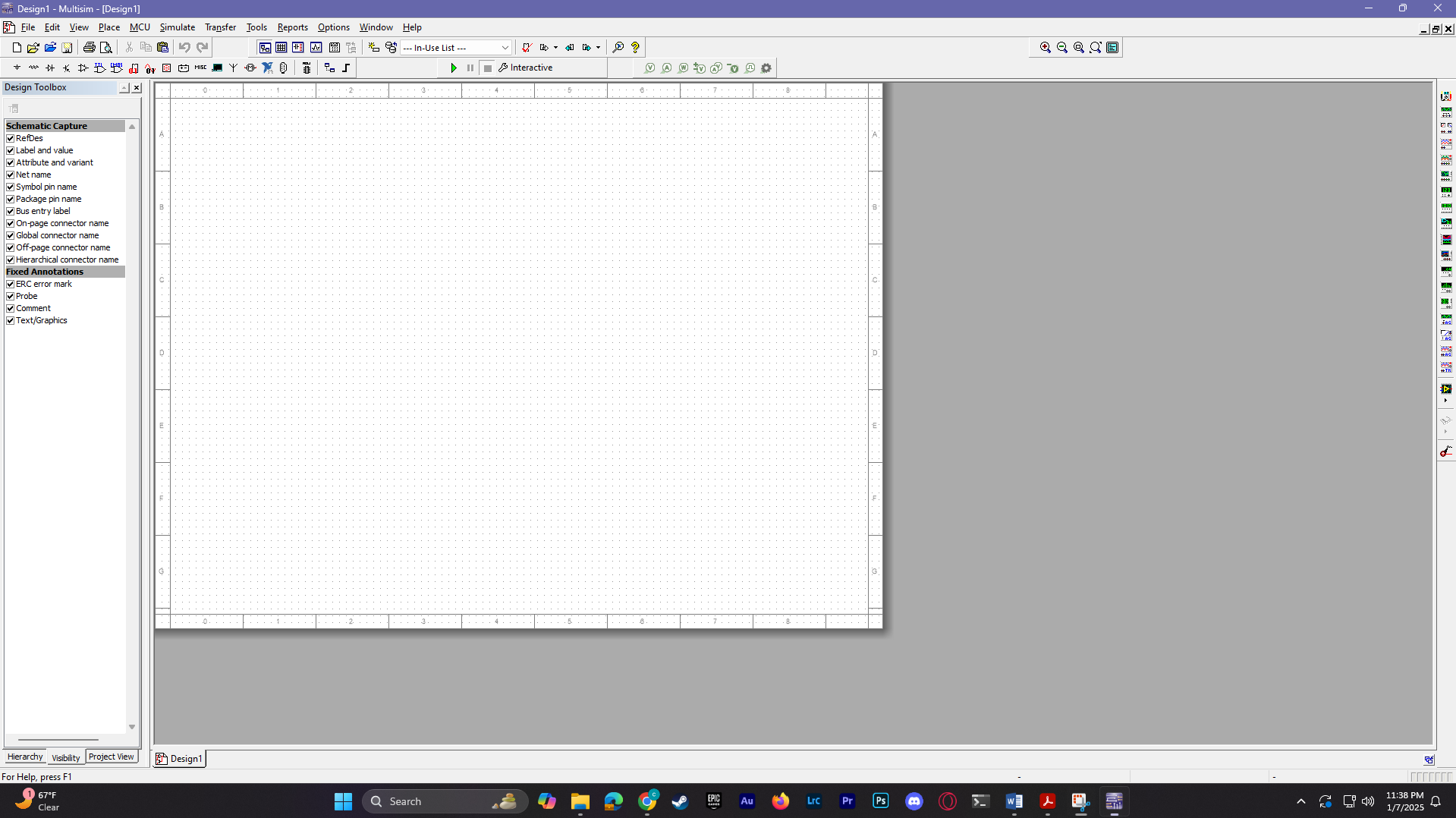
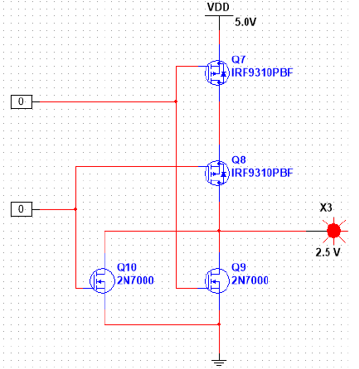


Fig.6 CMOS NOR Gate



Simulation: CMOS NOR Gate

**Results and Discussions:**

The primary objective of this experiment was to construct and characterize MOSFET logic gates, including NAND, NOR, and basic gates, and to enhance the understanding of MOSFET-based digital circuit design. Through systematic assembly and testing, we successfully demonstrated the operation of n-channel enhancement mode MOSFETs and their application in CMOS logic circuits. The experiment provided practical insights into the functionality of these devices, particularly their ability to switch states based on gate voltage and their use in constructing logic gates with complementary MOSFETs.

We saw expected outputs from the logic gates, verifying that the gates performed correctly under ideal conditions. For instance, the CMOS inverter consistently produced logic inversion with high noise immunity and low power dissipation, as predicted.

**Success of the Experiment**  
The experiment effectively met its goal of exploring MOSFET logic gates and their design principles. The findings confirmed the benefits of CMOS technology, such as low static power consumption, high noise immunity, and scalability, making it suitable for modern digital circuit applications. Moreover, the use of n-channel enhancement mode MOSFETs was successfully demonstrated, highlighting their importance in constructing efficient and reliable circuits. However due to time constraint we couldn’t complete one of the diagrams, particularly CMOS NAND gate. Otherwise everything else was a success.

**Mistakes and Challenges**  
During the experiment, a few challenges were encountered:

1. **Connection Errors:** At times, incorrect wiring led to unexpected outputs, requiring additional troubleshooting and testing.
2. **No heatsink:** It almost burned the fingers when touching the hot MOSFETS due to lack of precautions.

**References:**

1. Thomas L. Floyd, *Digital Fundamentals*, 9th Edition, 2006, Prentice Hall.
2. Boylestad, Robert L., *Electronic Devices and Circuit Theory*, Pearson Education, 2009.